TOKYO INSTITUTE OF TECHNOLOGY AND FUJITSU CREATE WORLD'S FASTEST WIRELESS TRANSMISSION

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TOKYO – JAPAN. Fujitsu Laboratories and the Tokyo Institute of Technology, today announced its achievement to create hardware capable of the world's fastest wireless transmission speeds of 56Gbps. In an effort to further enlarge the capacity of wireless equipment, they have developed a CMOS wireless transceiver chip that can process signals at high speeds with little loss across a broad range of frequencies, from 72 to 100 gigahertz (GHz).

The new chip is part of an effort to further enlarge the capacity of wireless equipment. They also developed technology to modularise it. Tokyo Institute of Technology and Fujitsu Laboratories have now developed high-speed wireless transceiver technologies that use the millimeter-waveband (30-300 GHz), where there are few competing wireless applications, and which are capable of large-capacity communications. This technology makes it possible to have high-capacity wireless communications equipment that can be installed outdoors in applications where fiber-optic networks would be difficult to lay.

A 56 Gbps transceiver circuit of the chip was developed by Fujitsu Laboratories together with Socionext. They developed a new timing detection method that combines the functions of the circuit that compensates signal degradation that becomes prominent as communication speeds improve with some of the functions of the timing-detection circuit that determines the bit-value of input signals, reducing the number of circuits. As a result, they succeeded in developing a 56 Gbps transceiver circuit that achieves twice the speed as before without raising power consumption.

To reduce the power consumption of the CDR, Fujitsu Laboratories and Socionext have now developed a new timing error detection method. By analyzing waveforms after DFE calculation, Fujitsu Laboratories and Socionext discovered that they could detect whether the DFE's operational timing was early or late by comparing the results of the two DFE determination circuits in cases where three consecutive bits in the input signal were 100 or 011. This led them to develop a new timing detection method that only detects the timing when three consecutive bits of the incoming signal are 100 or 011.

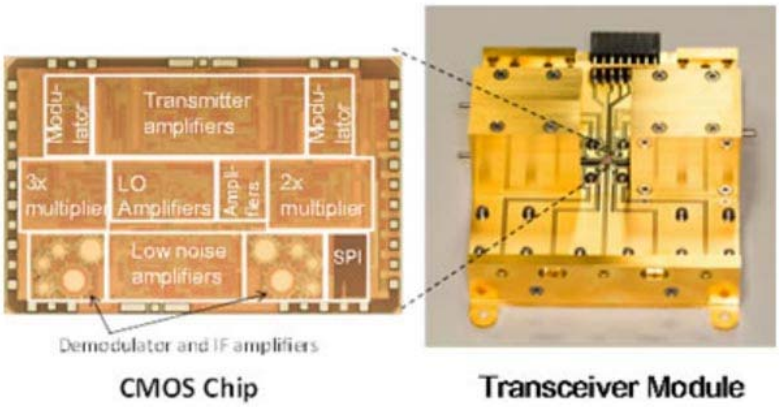

Fig.1 Transceiver CMOS chip and module.

With this newly developed timing detection method, the two companies were able to eliminate the previously required CDR incoming-signal timing-determination circuit, and lines, such as the clock line, which were required as the DFE and CDR operated with different timing. This made it possible for them to succeed in developing transceiver circuitry that doubles speeds to 56 Gbps with the same power consumption as before.

The result is, This new technology will be able to boost data transmission speeds between chips and optical modules without raising power consumption compared to the present. In addition, compatibility with upcoming OIF standards for optical module communications means that optical modules can be expected to be more compact and use less power, requiring half the number of transceiver circuits – from 16 to eight when using this technology – when constructing a 400 Gbps Ethernet with the current 28 Gbps standard.

It is envisioned that the Fujitsu Laboratories and co-developer Socionext's tech will appear in next-gen servers and switches. Interface components featuring the newly developed technology are expected to be commercialised from fiscal 2018 onwards. The details of this technology will be announced at the IEEE

International Solid-State Circuits Conference 2016 (ISSCC 2016), the largest conference related to semiconductor technology, held from January 31 in San Francisco.

Comments

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