Tokyo Institute of Technology and Socionext Inc. Announce World's Smallest Digital PLL, Opening the Door to Advanced System-on-Chip Technology

"Fractional-N PLL" Ideal for New Generations of AI, 5G, IoT Applications

TOKYO and SANTA CLARA, Calif., and February 10, 2020 --- Scientists at Tokyo Institute of Technology (Tokyo Tech) and Socionext Inc. have designed the world's smallest all-digital phase-locked loop (PLL), the two organizations announced today. All-digital PLLs enable new, high-performance system-on-chip (SoC) devices to serve emerging artificial intelligence, 5G cellular communications, and Internet-of-Things applications.

Reducing digital PLL size and improving performance is a significant step in enabling these next-generation applications, and creating a pathway to an SoC that can be fabricated in a small, 7-nm form factor, and in the coming generation of 5-nm technology.

Easy to Adopt Fractional-N PLL for Miniaturized ICs

As a core building block of SoC devices, the PLL synchronizes with the frequency of a reference oscillation and outputs a signal with the same or higher frequency, to provide a precise timing reference for the harmonious operation

PLLs require analog components that are bulky and difficult to scale down; digital PLLs eliminate those restructions.

Scientists at Tokyo Tech and Socionext Inc., led by Prof. Kenichi Okada, implemented a ‘synthesizable’ fractional-N PLL, which requires only digital logic gates, making it easy to adopt in conventional miniaturized integrated circuits.

Okada and the team used several techniques to minimize the required area of the synthesizable PLLs, including power consumption and jitter, which is defined as the unwanted time fluctuation when transmitting digital signals. To decrease the required footprint, the design team employed a compact ring oscillator that can be easily scaled down. To suppress jitter, they reduced the phase noise (random fluctuations in a signal) of the ring oscillator, using ‘injection locking’, which is the process of synchronizing an oscillator with an external signal whose frequency, or multiple of it, is close to that of the oscillator. This was achieved over a wide range of frequencies. The lower phase noise, in turn, enables reduced power consumption.

According to Professor Okada, the design of the synthesizable PLL is superior to all other current state-of-the-art PLLs because it achieves the best jitter performance with the lowest power consumption and the smallest area (see Figure 1). “The core area is 0.0036 mm^2, and the whole PLL is implemented as one layout with a single power supply,” said Okada. Also, it can be built using standard digital design tools allowing for rapid, low-effort, and low-cost production, making it commercially viable.

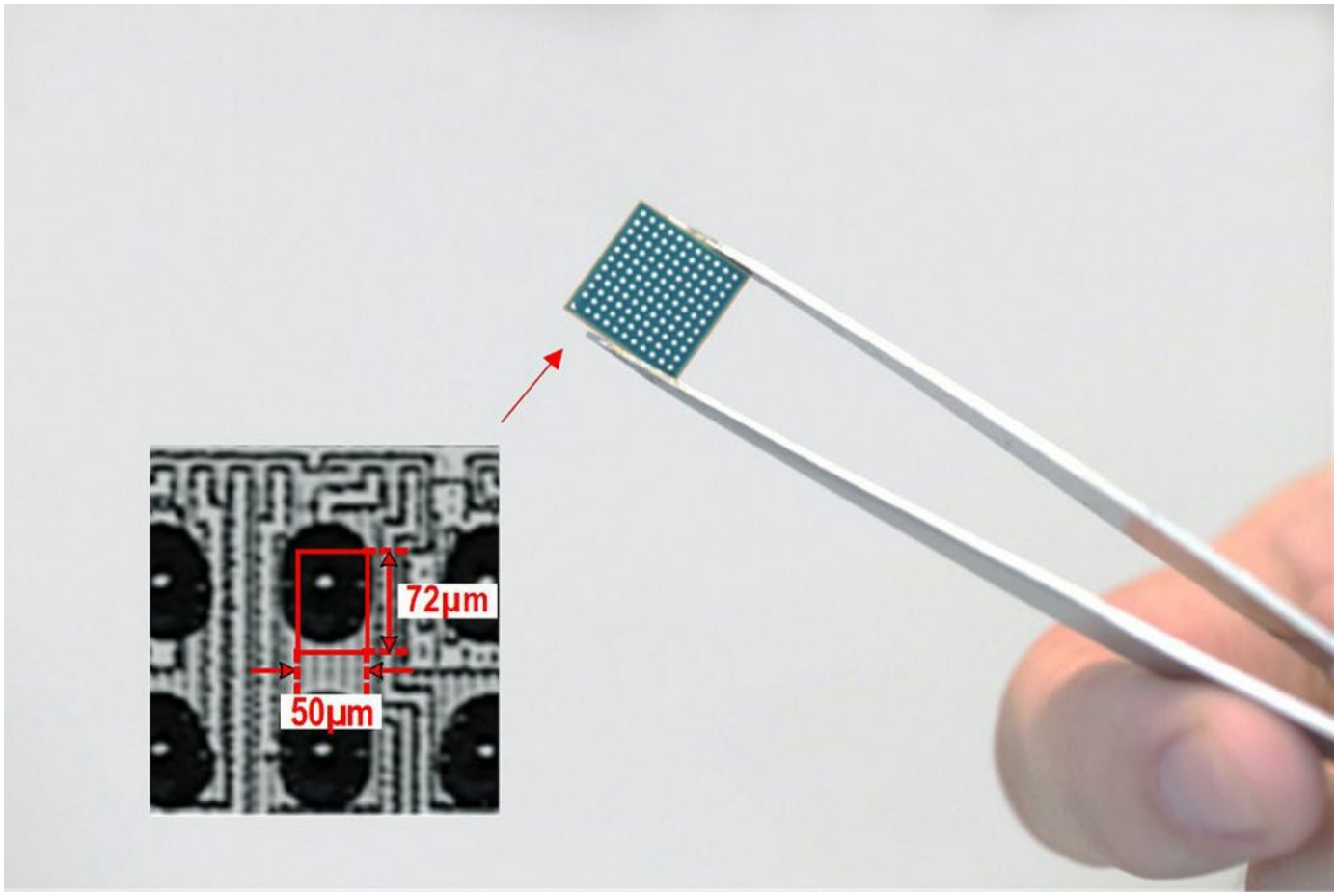

Figure 1. Photograph of a chip containing the proposed PLL
The entire all-digital PLL fits in a 50 × 72 µm2 region, making it the smallest PLL to date.

The synthesizable PLL can be easily integrated into the design of all-digital SoCs, making it valuable for developing the next-generation 5-nm semiconductor technology, an important factor for 5G, artificial intelligence, Internet of Things and other applications where high performance and low power consumption are critical.

Potential of Synthesizable Circuits

The contributions of this research go beyond these possibilities. “Our work demonstrates the potential of synthesizable circuits,” said Okada. “With the design methodology employed here, other building blocks of SoCs, such as data converters, power management circuits, and wireless transceivers, could be made synthesizable as well. This greatly boosts design productivity and can reduce design efforts.”

Tokyo Tech and Socionext will continue their collaboration in this field to advance the miniaturization of electronic devices, enabling new technologies.

The research work was conducted in cooperation with TeraPixel Technologies Inc.

Reference

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“monotsukuri,” meaning “technical ingenuity and innovation,” the Tokyo Tech community strives to contribute to society through high-impact research. www.titech.ac.jp/english/

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Tokyo Institute of Technology and Socionext Inc. Announce World’s Smallest Digital PLL, Opening the Door to Advanced System-on-Chip Technology

Introducing the world’s smallest all-digital phase-locked loop (PLL) designed by Tokyo Institute of Technology (Tokyo Tech) and Socionext Inc. enabling new, high-performance system-on-chip

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