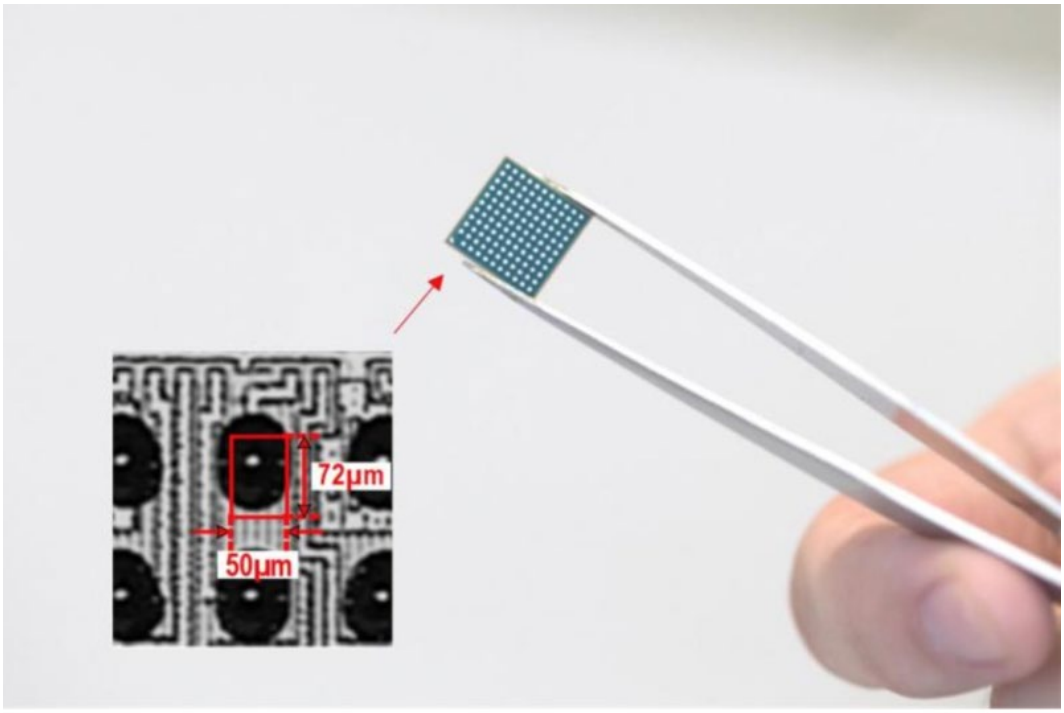
Electronics

Shrinking the phase-locked-loop for 5G

by Spencer Chin | Feb 10, 2020 3:44pm



The entire all-digital PLL fits in a 50 × 72 µm2 region, making it the smallest PLL to date. (Kenichi Okada, Tokyo Institute of Technology)

Phase locked loop circuits play a vital role in clock signaling for digital applications. However, they have up to now been relatively large devices comprising bulky analog components. Scientists at Tokyo Institute of Technology (Tokyo Tech) and Socionext Inc. have designed the world's smallest all-digital phase-locked loop (PLL)—a potentially timely development for 5G cellular communications, artificial intelligence, IoT, and other computationally-intensive applications.

PLL circuits are a core building block of SoC devices, as they generate clocking signals whose oscillations act like a metronome to provide a precise timing reference for the harmonious operation of digital devices. Designing an all-digital PLL is highly desirable as higher performance can be achieved with a smaller device. The Tokyo Tech and Socionext Inc. researchers, led by Prof. Kenichi Okada, achieved this goal by implementing a 'synthesizable' fractional-N PLL, which only requires a digital logic gate and no bulky analog components.

Okada and team helped achieve space savings by employing a ring oscillator that can be easily scaled down. To suppress jitter, they reduced the phase noise—random fluctuations in a signal—of this ring oscillator, using 'injection locking'—the process of synchronizing an oscillator with an external signal whose frequency (or multiple of it) is close to that of the oscillator—over a wide range of frequencies. The lower phase noise, in turn, reduced power consumption.

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"The core area is 0.0036 mm^2, and the whole PLL is implemented as one layout with a single power supply," remarks Okada. The device can be built using standard digital design tools, allowing for its rapid, low-effort, and low-cost production, making it commercially viable.

The researchers said that synthesizable PLL can be easily integrated into the design of all-digital SoCs, making it valuable for developing the much sought after 5nm semiconductor for cutting-edge applications. But the scientists see other benefits. "Our work demonstrates the potential of synthesizable circuits. With the design methodology employed here, other building blocks of SoCs, such as data converters, power management circuits, and wireless transceivers, could be made synthesizable as well. This would greatly boost design productivity and considerably reduce design efforts," explained Okada.

Tokyo Tech and Socionext will continue their collaboration to advance the miniaturization of electronic devices, enabling the realization of newer-generation technologies.

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