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A more accurate, low-cost 39 GHz beamforming transceiver for 5G communications

Tokyo, June 3, 2019 - Researchers at Tokyo Institute of Technology and NEC Corporation, Japan, present a 39 GHz transceiver with built-in calibration for fifth-generation (5G) applications. The advantages to be gained include better quality communications as well as cost-effective scalability.

CMOS chips on an 18 mm × 163.5 mm evaluation-board

A team of more than 20 researchers at Tokyo Institute of Technology (Tokyo Tech) and NEC Corporation has successfully demonstrated a 39 GHz transceiver that could be used in the next wave of 5G wireless equipment, including base stations, smartphones, tablets and Internet-of-Things (IoT) applications.

Although research groups, including the current team, have until now largely focused on developing 28 GHz systems, 39 GHz will be another important frequency band for

realizing 5G in many parts of the world.

The new transceiver (shown in **Figure 1**) is based on a 64-element (4 × 16) phased-array[1] design. Its built-in gain phase calibration means that it can improve beamforming[2] accuracy, and thereby reduce undesired radiation and boost signal strength.

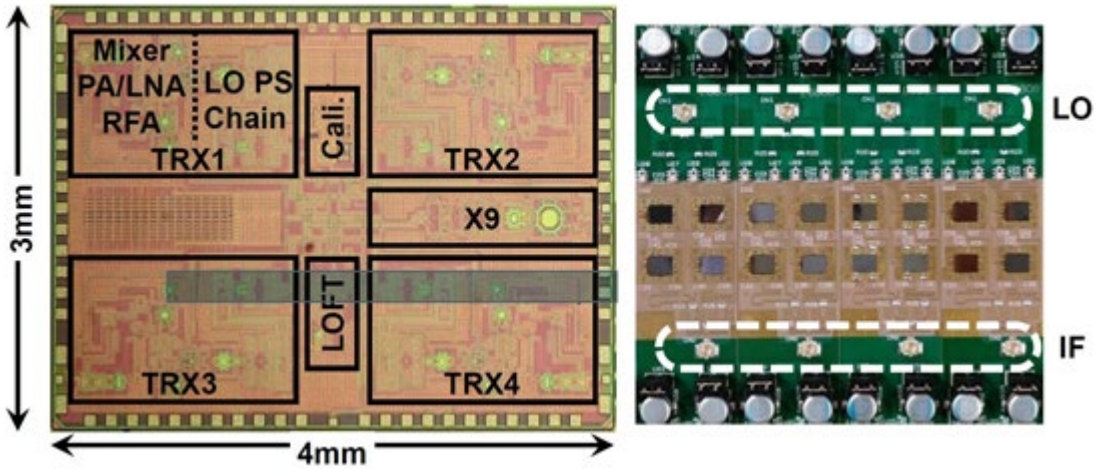

Figure 1. A micrograph of the chip and the 64-element module

The transceiver, based on a 64-element phased-array design, takes up a chip area of 12 mm^2

Fabricated in a standard 65-nanometer CMOS[3] process, the transceiver's low-cost silicon-based components make it ideal for mass production — a key consideration for accelerated deployment of 5G technologies.

The researchers showed that the built-in calibration has a very low root-mean-square (RMS) phase error of 0.08°. This figure is an order of magnitude lower than previous comparable results. While transceivers developed to date typically suffer from high gain variation of more than 1 dB, the new model has a maximum gain variation of just 0.04 dB over the full 360° tuning range.

"We were surprised to achieve such a low gain variation when actually using the calibration based on our local-oscillator (LO) phase-shifting approach," says project leader, Kenichi Okada of Tokyo Tech.

In addition, the transceiver has a maximum equivalent isotropic radiated power (EIRP)[4] of 53 dBm. This is an impressive indication of the output power of the 64 antennas, the researchers say, particularly for low-cost CMOS implementation.

Indoor testing (under anechoic chamber conditions[5]), which involved a one-meter, over-the-air measurement, demonstrated that the transceiver supports wireless transmission of a 400 MHz signal with 64QAM.

"By increasing the array scale, we can achieve greater communication distance," Okada says. "The challenge will be to develop the transceiver for use in smartphones and base stations for 5G and beyond."

This work is being presented at the 2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC) in Boston, Massachusetts, US, as part of the morning session (Session RTu2E) to be held on 4 June 2019. The paper of this work "A 39GHz 64-

Element Phased-Array CMOS Transceiver with Built-in Calibration" by Yun Wang et al., received the best student paper award.

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Technical terms

1. phased-array: Referring to an electrically steerable array of antennas.
2. beamforming: A powerful signal processing technique used to control antenna patterns.
3. CMOS: Complementary metal–oxide–semiconductor, the main processing method for creating integrated circuits.
4. Equivalent isotropic radiated power (EIRP): A measure of the signal strength or output power of an antenna in decibels per meter (dBm).
5. anechoic chamber conditions: A non-reflective environment that is designed to be free from echoes.

References

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