Tokyo Tech slashes power consumption in Bluetooth Low-Energy transceiver by more than half

Eying future of IoT

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TOKYO, Feb. 11, 2018 /PRNewswire/ -- **Researchers at Tokyo Institute of Technology (Tokyo Tech) announce a Bluetooth Low-Energy transceiver with the lowest ever power consumption - a breakthrough set to accelerate widespread adoption of Internet of Things (IoT) applications in Japan and around the globe.**

An ultra-low-power Bluetooth Low-Energy transceiver designed for use in the popular 2.4 GHz band has been developed by a group of researchers led by Kenichi Okada of Tokyo Institute of Technology, Japan.

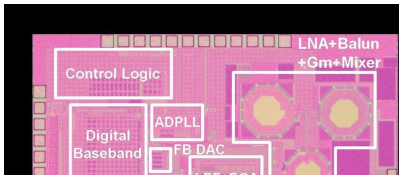

Figure 1. A photograph of the chip. The chip was designed using standard 65-nanometer CMOS technology.

When transmitting, the transceiver consumes 2.9 milliwatts (mW) and when receiving, it consumes just 2.3 mW. Given that minimizing power consumption is a requirement for the oncoming IoT era, these figures are remarkable, as they represent less than half the power consumed by previous transceiv

(see Table 1).

Why BLE matters

Within the next decade, IoT is projected to become a multi-trillion US dollar industry. Bluetooth Low-Energy (BLE) is in the spotlight as a key technology spurring the growth of this fast-evolving market. Already embedded in millions of Apple and Android devices, BLE is the most used short-range wireless technology aimed at low-power and low-cost connectivity.

Low-energy solutions are in demand not only for smartphones and watches, but also for emerging applications in the medical and healthcare fields, factories and public infrastructure such as roads, bridges and tunnels. IoT sensors for early detection and warning systems could mean the difference between life and death.

"Our research grew out of this need for connectivity," explains Okada. "In an IoT world, trillions of devices will be used. To extend battery life and aim for maintenance-free operations, reducing power consumption is vital."

Key features

The BLE transceiver has excellent receiver sensitivity[1] and high interference tolerance[2], while also realizing the lowest power consumption.

The transmitter employs an all-digital phase-locked loop (ADPLL), an attractive building block for BLE, as it is less susceptible to noise compared to its analog counterpart. The transceiver was designed in a 65-nanometer CMOS process[3].

In another study focusing on ADPLL, the researchers achieved a figure of merit[4] (FoM) of -246dB, one of the best obtained so far. The FoM is an important metric for evaluating the trade-off between performance and power consumption.

The above results arose from a project supported by Japan's New Energy and Industrial Technology Development Organization (NEDO).

Looking ahead

In future, Okada says: "The PLL could operate on just 0.65 mW, and studies are underway to reduce our transceiver's power consumption even further."

The team will present their findings at the 2018 International Solid-State Circuits Conference (ISSCC). Held every February in San Francisco, the conference, popularly known as the Chip Olympics, is regarded as the leading forum on integrated circuit research and development.

Table 1. A performance comparison of BLE transceivers

	Tokyo Tech ISSCC 2018	Renesas ISSCC 2015	Dialog ISSCC 2015	Texas Instruments CC2540	Nordic nRF51822
Transmitter	2.9	7.7	10.1	63	32
Receiver	2.3	6.3	11.2	58	39

Caption: Tokyo Tech's BLE transceiver achieves a dramatic reduction in power consumption - down to less than half of those previously reported. All figures are in milliwatts (mW).

Technical terms

[1] Receiver sensitivity: A measure of how well a receiver can pick up the tiniest of signals. The figure reached in this study was an impressive -94 decibels relative to 1 milliwatt (dBm).

[2] High interference tolerance: Referring to the need for high tolerance to interference from other signals operating in the busy 2.4 GHz band.

[3] CMOS process: A standard method of building integrated circuits using silicon-based complementary metal-oxide-semiconductor (CMOS) technology.

[4] Figure of merit (FoM): The FoM evaluates the trade-off between jitter (related to noise in wireless communication) and power consumption. Reducing jitter is desirable for improving the quality of communication, but this requires more energy, so there is a trade-off between performance and power consumption. In general, the lower the FoM, the better. The figure of -246dB is one of the lowest ever achieved.

Reference

Title: A 0.98mW Fractional-N ADPLL Using 10b Isolated Constant-Slope DTC with FOM of -246dB for IoT Applications in 65nm CMOS
Authors: Hanli Liu, Dexian Tang, Zheng Sun, Wei Deng, Huy Cu Ngo, Kenichi Okada, Akira Matsuzawa

Affiliation: Tokyo Institute of Technology, Tokyo, Japan

Title: An ADPLL-Centric Bluetooth Low-Energy Transceiver with 2.3mW Interference-Tolerant Hybrid-Loop Receiver and 2.9mW Single-Point Polar Transmitter in 65nm CMOS
Authors: Hanli Liu, Zheng Sun, Dexian Tang, Hongye Huang, Tohru Kaneko, Wei Deng, Rui Wu, Kenichi Okada, Akira Matsuzawa
Affiliation: Tokyo Institute of Technology, Tokyo, Japan

Both papers have been selected for presentation at the 2018 IEEE International Solid-State Circuits Conference (ISSCC).

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https://www.titech.ac.jp/english/research/stories/faces8_okada.html

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