Clock generator realized by pure digital circuit

Research

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Summary

A research group including Professor Akira Matsuzawa and Associate Professor Kenichi Okada, of the Graduate School of Science and Engineering at the Tokyo Institute of Technology, succeeded in manufacturing a new kind of clock generator realized by a pure digital circuit. They did so by stable use of "injection-locking," where an oscillator oscillates after synchronizing with an injected signal, and by carrying out phase locking through feed-forward control. In conventional clock generator circuits, exact phase locking through feed-back control was required, so they couldn't be implemented by digital circuits. The new clock generator circuits had their prototypes made using a silicon CMOS process with minimum manufacturing dimensions of 65 nanometers, and are able to generate a clock at 0.4G-1.4GHz (gigahertz, 1GHz is 1,000,000,000 hertz), and have extremely low power consumption at 0.78mW for 0.9GHz output. This was achieved at tiny dimensions of 0.0066mm^2. Almost all integrated circuits need a clock generator circuit, and if this new clock generator circuit is used then ultra-small battery-less sensors will be able to be incorporated in all kinds of mobile devices.

This research result was presented on the 11th of February at the ISSCC (International Solid-State Circuits Conference) held in San Francisco starting on the 9th of February, 2014.

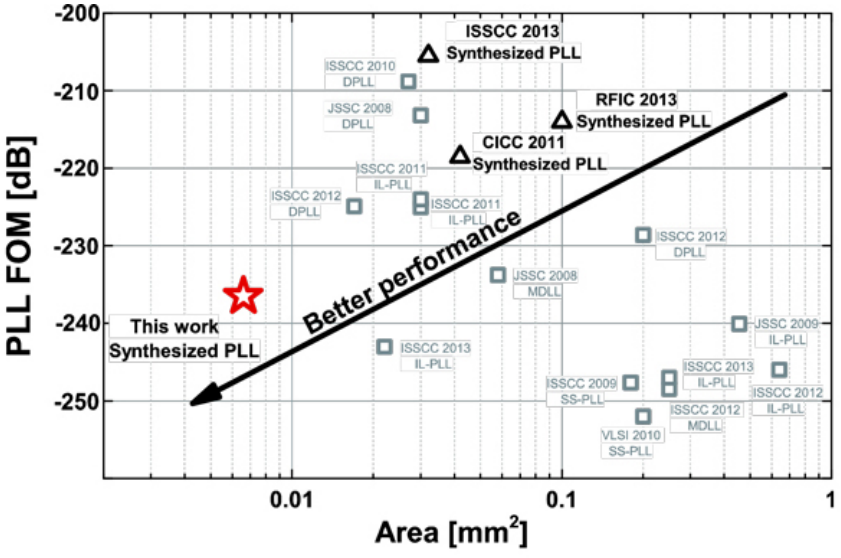

Figure Comparison of thesis data and performance

Features: In a comparison with the latest research results reported at international conferences, large-scale miniaturization and jitter-minimization have been realized. The grey items are manual-designed PLL, while the black items are automatically designed PLL. The star shaped PLL from the current research results can be automatically synthesized as digital circuits, so they have realized large-scale miniaturization and low power consumption.

Reference

Authors: Wei Deng, Dongsheng Yang, Tomohiro Ueno, Teerachot Siriburanon, Satoshi Kondo, Kenichi Okada, Akira Matsuzawa

Title: A 0.0066mm^2 780μW fully synthesizable PLL with a current-output DAC and an interpolative phase-coupled oscillator using edge-injection technique

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