Best Student Design Awards Presented at ISSCC 2007

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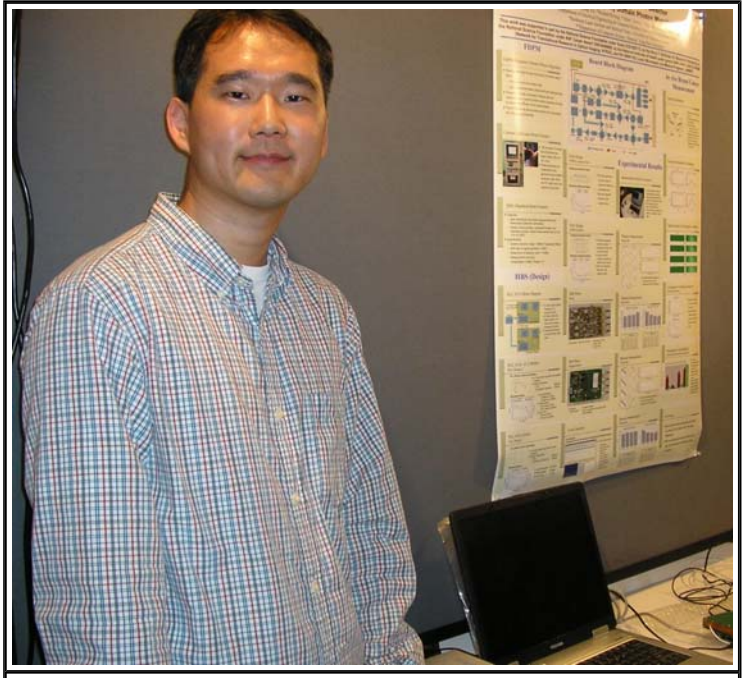
The winners of the DAC and A-SSCC Student Design Contests of 2006 presented their work in two evening poster sessions at ISSCC 2007 in San Francisco.

The A-SSCC prize winners were honored at the conference in November, 2006. The DAC awardees will be formally acknowledged at the 44th Design Automation Conference in San Diego, California in June, 2007.

48 papers were submitted from 15 countries for the ten DAC awards. “This was an excellent year,“ said Bill Bowhill, a Co-Chair of the contest. “The winners have outstanding designs. Many of the students showed demonstrations of their designs at the conference which generated much interest from the attendees.”

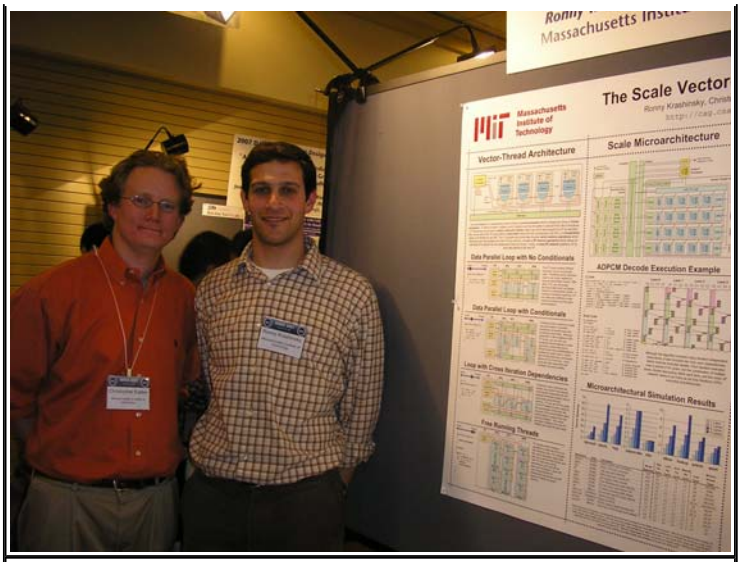
Award-winning projects were not ranked for the first time this year due to past difficulties in comparing papers dealing with very different topics and/or technologies. There was also no clear outstanding paper for “best overall,” said Kaushik Roy, DAC Design Community Chair. "Since many EMS/sensors and ADC papers were submitted this year, more support from Data Converters and Sensor ISSCC committees will be added next year," he said. The DAC student contest is restricted to designs originating in university undergraduate or graduate course work or research.



Keun Sik No of UC Irvine explained that his hand-held breast cancer detector “can actually see the inside contents of the tissue,” unlike xray mammograms and MRI’s. In post-doc work he plans to make the device smaller and cheaper so it can be used by patients at home as often as every hour or half hour to monitor the progress of chemotherapy. Mr. No said he has been interested in electronics “ever since I was a kid.”

The body sensor processor devised by Sungdae Choi, an A-SSCC award winner, can be used at home for monitoring and transmitting bio-signals to health care professionals. He envisions that with this device “even healthy people will be able to catch symptoms of abnormal health conditions” and have them automatically forwarded for follow-up.

“When I was very young, I was interested in making something work as I desired,” he said. “So I decided in my mind to become a doctor, a kind of doctor. I wanted to contribute to human life. My dream came true. Now I have another dream, to make some useful gadget for people and every person will use the gadget I made.”



"Vector-threaded architecture is able to exploit both data parallel vector computation and act as a highly multi-threaded engine," said designer Ronny Krashinsky of MIT (at right). “We wanted to find a flexible architecture that could execute many different types of embedded applications like graphics, network processing, and cryptography.”

“The basic interface to the architecture is virtual processors; each typically executes one iteration of a loop,” he said. “If it’s a vectorizable loop, it’s executed purely with vector instructions. But if the loop has conditional operations, then each of those virtual processors can take a conditional branch to direct their own control flow. So the overhead of repeatedly executing blocks of instructions gets amortized.”

Christopher Batten (at left), who created the high bandwidth memory system to support Krashinsky’s execution unit, said, “I always wanted to do hardware - chip design. When I came to MIT, I thought we’d be doing chips right away. But it took six years before we actually built a chip. That took about two years, but it was worthwhile because a lot of our initial area and energy claims were validated by doing it.”

This was a very small-scale project, Batten said. “Two students, less expensive, very hands on. We got to do everything. It was a lot of fun.”

“One of the cool things about doing this is that I get to come to ISSCC,” he concluded. “It’s so different from the conferences I go to. There’s a whole lot more industry people here. It’s a whole different community.”

CHIP/SYSTEM OPERATIONAL

A Wireless Implantable Microsystem for Continuous Blood Glucose Monitoring

Mohammad M Ahmadi, Graham A Jullien
University of Calgary, Canada

An amperometric glucose sensor, transpondor chip in 0.18um CMOS technology and external receiver are presented. The implantable sensor and transponder design supporting load modulation demonstrated promising performance: 132uA with 6bit accuracy.

SYSTEM OPERATIONAL CATEGORY

HBS: a Handheld Breast Cancer Detector Based on Frequency Domain Photon Migration

Keun Sik No et al.
University of California Irvine, USA

This paper presents a non-invasive handheld breast cancer detector using frequency domain photon migration spectroscopy. The receiver is in heterodyne topology and detects broadband-modulated (10MHz – 1GHz) signal. A performance similar to that of laser based system is demonstrated

CHIP OPERATIONAL CATEGORY

Design of an Ultra-Low-Voltage UWB Baseband Processor
Vivienne Sze, Anantha Chandrakasan,Massachusetts Institute of Technology, USA

A 100Mbps throughput UWB baseband processor operating at a sub-threshold supply voltage of 0.4V is presented. This work demonstrates the application of sub-threshold design to high performance systems using parallelism.

An Energy-Efficient Reconfigurable Multiprocessor IC for DSP Applications
Guichang Zhong, Alan N Wilson, University of California, Los Angeles, USA

This work presents a low-power reconfigurable multiprocessor with a performance close to ASIC solutions while possessing a degree of flexibility.

A 94dB SFDR 78dB DR 2.2MHz BW Multi-bit Delta-Sigma Modulator with Noise Shaping DAC
Jianzhong Chen, Yong Ping Xu, National University of Singapore, Singapore

The work presents a multi-bit low-pass delta-sigma modulator employing a noise shaping dynamic matching technique that improves both SFDR and SNR.

A 230mV-to-500mV 375KHz-to-16MHz 32b RISC Core in 0.18µm CMOS
Chen Jian-Shiun, Yi-Ming Wang, Yu-Juey Chang, Jinn-Shyan Wang, Chingwei Yeh, Tien-Fu Chen, National Chung-Cheng University Taiwan R.O.C

This work presents a low supply voltage, 230-500mV, RISC core with 375KHz-1MHz clock frequencies. The ultra-low voltage CMOS technique such as dynamic NP-swappable body bias scheme is extensively studied.

A 152mW/195mW Multimedia Processor with Fully Programmable 3D Graphics and MPEG/H.264/JPEG for Handheld Devices
Jeong-Ho Woo, Ju-Ho Sohn, Hyejung Kim, Jongcheol Jeong, Euljoo Jeong, Suk Joong Lee, Hoi-Jun Yoo, KAIST, South Korea

This work presents a multimedia SoC including MPEG4 codec, H.264 decoder, JPEG codec, and fully programmable 3D graphics engine. The proposed JPEG/MPEG hybrid design provides small area and low power design. The SoC consumes 152mW at 48MHz operating frequency.

A 252Kgates/4.9Kbytes SRAM/71mW Multi-Standard Video Decoder for High Definition Video Applications
Chih-Da Chien, Chien-Chang Lin, Yi-Hung Shih, He-Chun Chen, Chih-Wei Wang, Cheng-Yen Yu, Chih-Liang Chen, Ching-Hwa Cheng, Jiun-In Guo, National Chung-Cheng University Taiwan R.O.C., Feng-chia University Taiwan R.O.C.

This paper presents a multi-standard video decoder supporting JPEG, MPEG-1,2,4, and H.264 for HD video applications. Active hardware sharing scheme and techniques that can reduce memory bandwidth are proposed. The chip consumes71.1mW at 120MHz/1V and 7.9mW at 20MHz/0.8V.

A 152mW/195mW Multimedia Processor with Fully Programmable 3D Graphics and MPEG/H.264/JPEG for Handheld Devices
Jeong-Ho Woo, Ju-Ho Sohn, Hyejung Kim, Jongcheol Jeong, Euljoo Jeong, Suk Joong Lee, Hoi-Jun Yoo, KAIST, South Korea

This work presents a multimedia SoC including MPEG4 codec, H.264 decoder, JPEG codec, and fully programmable 3D graphics engine. The proposed JPEG/MPEG hybrid design provides small area and low power design. The SoC consumes 152mW at 48MHz operating frequency.

CONCEPTUAL [functional silicon shown at conference]

The Scale Vector-Thread Processor
Ronny Krashinsky, Christopher Batten, Krste Asanovic, Massachusetts Institute of Technology, USA

This work presents the scale vector-thread processor as a complexity-effective solution for embedded computing. An efficient design flow and low power design techniques are thoroughly explored. It demonstrates the potential performance of the vector-thread unit.

The A-SSCC posters were:

A 1.5 MS/s 6-bit ADC with 0.5V Supply
Simone Gambini, Jan Rabaey, UC Berkeley

A TCAM-based Periodic Event Generator for Multi-Node Management in the Body Sensor Network
Sungdae Choi, Kyomin Sohn, Jooyoung Kim, Jerald Yoo, Hoi-Jun Yoo, Kaist, Daejeon Korea

A 0.98 to 6.6 GHz Tunable Wideband VCO in a 180 nm CMOS Technology for Reconfigurable Radio Transceiver
Tusaku Ito, Hirotaka Sugarawa, Kenichi Okada, Kazuya Masu, Tokyo Institute of Technology

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