Second A-SSCC Considers Challenges for the e-Life

Gathered for the opening plenary of the A-SSCC in Hangzhou are(l-r) Prof Tadahiro Kuroda of Keo University and Chair of the Invited Program Committee, Nicky Lu of Etron Technology and Chair of Conference Industry Program, Richard C. Jaeger of Auburn University and President SSCS, Richard Chang, the President of Semiconductor Manufacturing International Corporation and Chair of the Technical Program, and C.K. Wang of National Taiwan University and Conference Steering Committee Chair.

The successful Asian Solid-State Circuits Conference in November, 2006 in Hangzhou, China was organized with a core of 107 papers selected by an international program committee. The acceptance rate was 32% with a conference audience of 260 registered attendees. CK Wang, the Steering Committee chair of A-SSCC reported that the conference was quite successful both "in terms of paper quality and foreign attendees with 82 from Japan, 48 from Taiwan, and 39 from Korea." Prof Wei of Tsinghua Univ and local host felt that it was the first high quality and world class conference held in China. The tutorials that began the conference, were open at no cost to any students in attendance.

Three papers, announced as winners of the Student Design Contest, were awarded at A-SSCC. The competition, in cooperation with the ISSCC, includes transportation for the lead student researcher to the ISSCC February 2007 in San Francisco, for the papers to be included in the ISSCC poster session. The A-SSCC student design contest finalists are selected from regular accepted papers that are authored by students. Only the good real designs, not simply simulations, are selected and invited to demonstrate the operation of the chips on-site. It is not a contest with a single specification or application, but rather a contest for the completeness of developing and demonstrating a fabricated integrated circuit design. The papers, co-authors, and abstracts are listed below.

Winners of the A-SSCC 2006 student design contest were (from left) Sungdae Choi of KAIST, Seoul, Mr. Yusaku Ito of the Tokyo Institute of Technology, and Mr. Simone Gambini of the University of California at Berkeley. Presenting the awards is Prof. Hoi-Jun Yoo, Chair of Design Contest.

(I) A TCAM-based Periodic Event Generator for Multi-Node Management in the Body Sensor Network

Sungdae Choi, Kyomin Sohn, Jooyoung Kim, Jerald Yoo andHoi-Jun Yoo (KAIST)

A low-power periodic events generation is essential for a node controller in the network system with centralized control and the timer interrupt generation for various devices in a CPU. The proposed TCAM-based periodic event generator manages the issuing events with the programmed value and the number of the events is equal to the number of the word line of the TCAM block. The NAND-type TCAM cell operates with as low as 0.6V supply voltage and the low-energy match line precharge reduces the search line transition which causes most of the search energy dissipation. The implemented event generator consumes 184-nJ energy to schedule events of 255 nodes for 24-hours, which is less than 10% of energy consumption of conventional hardware timer blocks.

(2)A 0.98 to 6.6 GHz Tunable Wideband VCO in a 180 nm CMOS Technology for Reconfigurable Radio Transceiver

Yusaku Ito, Hirotaka Sugawara, Kenichi Okada and Kazuya Masu (Tokyo Institute of Technology)

This paper proposes a novel wideband voltage-controlled oscillator (VCO) for multi-band transceivers. The proposed VCO has a core LC-VCO and a tuning-range extension circuit, which consists of switches, a mixer, dividers, and variable gain combiners with a spurious rejection technique. The experimental results exhibit 0.98-to-6.6GHz continuous frequency tuning with -206dBc/Hz of FoM_t which is fabricated by using a 0.18um CMOS process. The frequency tuning range (FTR) is 149%, and the chip area is 800µµm x 540µm.

(3)A 1.5MS/s 6-bit ADC with 0.5V supply

Simone Gambini and Jan Rabaey (University of California at Berkeley)

A moderate resolution analog-to-digital converter targeting wireless sensor networks applications is presented. Employing a successive-approximation architecture, the device achieves 6 bits of resolution at 1.5 MS/s output rate, while drawing 28 microamps from a low 0.5 V supply, corresponding to a Figure of Merit (FOM) of .25pJ/conversion step. Low-density metal5-metal6 capacitors guarantee feedback DAC linearity while minimizing input capacitance, while the use of a passive sample and hold, combined with a class-AB comparator reduce analog power dissipation to 4 microWatts (30% of the total). The analog core is operational for supply values as low as .3V, even though sampling rate is reduced to 175kS/s.

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